# Project description:

## Background

### State of the art:

Hot science topic today is realization of quantum computer. Main advantage of quantum computer is solving specific classes of algorithms orders of magnitudes faster than classical computer.

Classical computer is based on deterministic two level states cells called bits. Quantum computer is also based on two level states (basis states) units call quantum bits (qubits). Qubit unlike classical bit exploits quantum phenomena of superposition which mean that it can be in any state between the basis ones.

There are several proposals for qubit implementation (below are listed just solid state implementations):

* Electrons on Helium (He) [1]
* Semiconductors:
  + - Nuclear spin qubits [2]
    - Electron (hole) spin qubits [3]
* Superconductors:
  + - Flux qubits [4]
    - Charge qubits [5]

As stated above, one of the qubit realizations in semiconductors is electron (hole) spin qubits.

In 1998 Loss and DiVincenzo came up with a proposal for scalable quantum computer for such a qubit and they developed the criteria [6] such a qubit should obey for quantum computer to work correctly.

Criteria for scalable quantum computer:

* identification of well-defined qubits
* reliable state preparation
* low decoherence (high coherence)
* accurate quantum gate operations (state manipulation) and
* strong quantum measurements (state readout)

Well defined qubit is a two level (two state) system whose levels are distinguishable and highly controllable. Qubit operation takes place by operating (manipulating) this two states.

Decoherence is phenomena of losing initially set qubit state and is characterized by characteristic time, in literature called coherence time T2 [2].

For all qubits it is desired to have coherence time as high as possible while gate operation (spin state manipulation) and measurement (state readout) as low as possible.

For a physical implementation of the two level system Loss and DiVincenzo proposed using charge particle (electron or hole) spin in a quantum dot (QD).

**What is a spin?**

Spin is intrinsic quantum mechanical property of every elementary particle. For electrons and holes it can take two states: spin-up and spin-down. In a magnetic field spin splits in two different energy levels related to spin-up and spin-down.

**What is a QD?**

For accessing and manipulating charge particle spin, one must confine it into the region, in size comparable to the charge particle wavelength in order to distinguish from other orbital energy levels. QDs are very small structures (diameters can reach tens of nanometers) and because of their almost zero dimensionality, possible energy levels for a charge particle are discrete and far away from each other. This fact has enabled the possibility of confining single charge particle on such a structure. By applying external magnetic field spin energy states splits in two and become distinguishable for manipulation and readout.

**DQD**

For achieving good state preparation, manipulation and measurement, additional mechanisms are required beyond ones offered by single QD. One of the most promising building block for realization of the spin qubit quantum computer based on quantum dots is serial double quantum dot (DQD) system. DQD system consists of two neighbouring quantum dots tunnel coupled to each other which means they can exchange charge particles by tunneling. Main physical property which makes them good is Pauli exclusion principle. It says that two identical fermions (in this specific case electrons or holes) cannot occupy same energy state. Two further principles are then based on this one: exchange interaction for spin manipulation and spin blockade for state readout.



Figure 1: Spin state readout based on spin blockade in gate defined electron DQD. Blue circles are individual quantum dots, white lines are gates. Black arrows in blue circles represent electron spin in left and right dot. Left to the DQD is charge sensor in form of quantum point contact. If there are two electrons on the right dot current through charge sensor does not flow otherwise it flows.

Figure 1 describes how spin blockade allows info about electron spin in the left QD in the DQD system. Info is collected by reading out a current through neighbouring charge sensor in form of quantum point contact (QPC). If spin configuration is like in Figure 1a) then after electrostatic pushing, by applying voltage pulses on gates L and R, both electrons finish on the right dot and current through charge sensor stops to flow, like show in Figure 1b). In the other case, Figure 1c), electrons on both dots have same spin and due to Pauli exclusion principle they stay in that configuration after electrostatic pushing. Consequently, current through charge sensor continues to flow.

**Materials**

Mostly used material for QD fabrication so far is **GaAs**. It has a drawback that electron spins in this material losses their coherence fast because of their coupling to the high number (~106) of gallium and arsenic nuclear spins trough the so called hyperfine interaction which manifests as noise added to externally applied magnetic field (nuclear noise). Initially measured coherence time T2 was 10 nanosecond [9]. By applying Hahn echo pulse sequence coherence time was boosted to 1.2 microsecond [9]. By further studying nuclear noise properties and applying techniques for nuclear notch filtering, F. Malinowski and F. Martins from group of Charles M. Marcus in Copenhagen has recently achieved coherence time of 0.87 millisecond in gate defined double quantum dot [7].

Silicon **Si** on the other hand is very promising because it can be isotopically purified and left with 29Si which is nuclear spin zero element, so nuclear noise can be very much reduced and coherence time boosted. Additional big advantage is compatibility with current CMOS technology. The later one should enable scalability which is inevitable property for reaching number of qubits required by quantum algorithms.

One way of defining QDs in silicon is by means of phosphorous P doping of specific Si crystal region. In that case phosphorous atom behaves as an electron quantum dot because of it confining potential. Andrea Morello Group from UNSW Australia, applying Hanh echo pulse sequence, has measured electron spin coherence time exceeding 200 microsecond, in non – isotopically purified Si:P system [3]. Using isotopically purified 28Si:P and nuclear spin of phosphorous atom as a qubit basis, the same group has achieved nuclear spin coherence time of 60 millisecond [2].

The major drawback in silicon is relatively weak spin orbit coupling for electrons what results in difficult spin manipulation via electric fields (described in more detail in *Research Methods*). The other way of defining QDs based on silicon platform, used in our group, is combining it with a germanium Ge [10]. Resulting material is called silicon germanium **SiGe**. Germanium is deposited on top of the silicon and difference in atomic distances in germanium and silicon crystal result in strain which relaxes creating quantum dots and nanowires in germanium part. Nanowires can be further electrostatically splitted in several QDs, forming double quantum dots or similar structures.

Holes in germanium **Ge** unlike electrons in **Si** have higher spin orbit coupling which together with keeping above mentioned advantages for electrons in silicon makes them promising spin qubit platform.

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Figure 2: SiGe nanowire based DQD sample fabricated in our group by Hannes Watzinger. Ohmic contacts labeled S (source) and D (drain) contacting thin withe nanowire (NW). Gate electrodes (G1 to G5) are on the top, isolated from the nanowire with 10nm hafnium oxide.

**In all spin qubit approaches above (and all qubits in overall) there is battle between spin manipulation time on one side and coherence time on the other side. For making a set of quantum operation correctly, manipulation time for one operation need to be much shorter than coherence time.**

Minimum time for one full spin rotation (longest single operation, π/2 spin rotation) in gallium arsenide double quantum dot system based on electron spin, J. Petta et al. achieved approximately 180 ps. They achieved coherence time, applying Hahn echo technique, T2 of 1.2 us (*this is strange – ratio T2 / π/2 seems too good*).

π/2 spin rotation achieved in Andrea Morello Group from UNSW Australia in Si:P material system, using ESR (electron spin resonance technique) is 75 ns [3]. Their T2 is 200 us [3].

Using hole spin in p-type silicon industrial CMOS as qubit basis, R. Maurand from S. De Franceschi group in CEA Grenoble, achieved π/2 spin rotation of approximately 3 ns [11]. While coherence time T2 in their case was 245 ns [11].

As mentioned above, reason for slow spin manipulation (long π/2 spin rotation) in case of silicon material system is low spin orbit coupling for holes and even lower for electrons, what can be seen from the measured results above. Holes in germanium have much higher spin orbit coupling leading to much faster spin manipulation in these type of qubits.

Measurement of the calculation result could be done by spin state projection on the basis states. Physically this is achieved using principle of Pauli spin blockade, as explained on Figure 1. Charge configuration then reveals the spin state. Charge configuration can be measured in several way as listed below.

Nowadays used techniques for qubit state sensing:

* DC current readout
* Differential measurement (AC current readout)
* Ohmic reflectometry
* Gate reflectometry

DC current readout is sensing the electron transport through the qubit by means of current measurement. It requires electron transport which in DQD system is not possible, so it requires additional charge sensor. It is prone to low frequency 1/f noise.

Differential measurement (AC current readout) has the same drawbacks as DC current readout. It is typically done with low frequency lock in technique.

Ohmic reflectometry is technique of indirect sensing of the change in a qubit impedance by monitoring amplitude or phase of the portion of the sent wave reflected from the qubit structure. It is usually done by high frequency lock in technique and is not prone to 1/f noise.

Gate reflectometry is technique of indirect sensing of the change in a qubit capacitance by monitoring amplitude or phase of the portion of the sent wave reflected from the one of the qubit gates. **It’s big advantage is that it does not require charge transport through the qubit.**

**What is reflectometry?**

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Figure 3: Basic principle of ohmic reflectometry. CS and RS constitutes equivalent electrical schematic of a measured sample, e.g. single electron transistor as charge sensor of DQD formed by single quantum dot. S and D denotes source and drain contacts of the charge sensor respectively. Resonance circuit formed with inductor L and capacitance C is connected to source contact.

Reflectometry is readout technique based on change of wave reflection coefficient Γ. It comes from electromagnetic wave principle – if the wave is travelling in media with impedance Z0  (e.g. coax cable) and it encounters change of impedance (e.g. coax end) to Z, portion of the wave will be reflected back according to the expression: , where Ar is amplitude of a reflected, Ain amplitude of an incoming wave and Γ is reflection coefficient.

Putting resonant circuit with incorporated charge sensor (Figure 3, red polygon) instead of coax cable end one can measure charge sensor impedance change caused by change in charge configuration in the nearby DQD. If elements of a resonant circuit – inductance L and capacitance C are properly chosen, on the resonant frequency of that circuit, , wave reflection coefficient Γ is minimized. Thus if DQD charge configuration changes -> charge sensor impedance changes -> reflection coefficient changes -> amplitude of reflection wave changes.

*Measurement need to be sensitive enough to achieve signal to noise ratio (SNR) high enough (typically SNR of more than 10) in a short time. Signal to noise ratio is the ratio of signal and noise amplitude in a given bandwidth. Measurement sensitivity is a measure of the change in an amplitude of current or amplitude (phase) of reflected wave when charge configuration is changed. Noise comes from 1/f noise on lower frequencies, intrinsic shot noise, thermal noise, noise in in measurement equipment… Lowering the measurement bandwidth (integration or filtering) noise is lowered and SNR raised but measurement become slower. Thus for achieving good SNR in short time signal need to be high. In our case fast measurement is required to obtain good quality measurement fast enough.*

### Definition of the problem:

As mentioned before DQD properties are defined by gates positioned on top of the nanowire (Figure 2). Static voltage on gates G1 and G2 creates potential wells forming double quantum dot system. For operating this DQD as a qubit it need to be isolated from the ohmic contacts, what is role of G3 and G5.

**Since the charge transport through DQD is forbidden, all readout techniques based on charge transport are not sensitive enough, for measurement to be fast enough – signal very small – integration time very large to achieve acceptable SNR. Readout techniques in this category are DC current readout, AC current readout and ohmic reflectometry.**

Usual solution to this problem is to place additional, separated quantum dot in form of single electron transistor or quantum point contact, called charge sensor (Figure 1), electrostatically coupled and thus sensitive to charge configuration in DQD. Charge sensor itself is well coupled to ohmic contacts thus it is suitable for charge transport measurements and ohmic reflectometry.

**Charge sensors suffer from conductance profile thermal broadening what lowers the sensitivity thus speed of readout. They also need additional compensation gates to substract the influence of the qubit gates on their conductance. Also, by looking into the future, for usable quantum processor qubit number needs to be scaled up to achieve big enough number required by quantum algorithms.** **Gate reflectometry does not suffer from previously listed problems and since it is using already defined electrostatic gates it does not need charge sensor, thus has a big potential to address scalability problem.** By usage of frequency division multiplexing all qubits in a quantum processor could be read out through a one (or several) wires.

Regarding current achievement in the gate reflectometry, M.F. Gonzalez – Zalba et al. reported charge sensitivity of 37 μeHz-1/2 using gate reflectometry on the gate strongly coupled to the silicon nanowire based DQD [12]. Reported result shows sensitivity almost the same as charge sensors (RF quantum point contact and RF single electron transistor) which is in μeHz-1/2 regime [12], but suffers from all the issues stated above.

### Proposal objectives:

Objectives of this proposal are to design **fast gate reflectometry** and perform **spin manipulation experiments** on a germanium based, hole spin double quantum dot.

For gate reflectometry, goal would be to achieve charge sensitivity comparable or even faster than reported in [12], which would enable obtaining quality measurement data (good SNR) fast enough and consequently allow to progress faster in creating spin qubit in this type of material.

After good readout technique is set up there is a series of experiment to be done to approach to the qubit realization. One of these is relaxation time measurement T1. Relaxation time T1 is the time during which charge particle spin stays in the prepared state. Spin manipulation experiments like measuring spin dephasing time T2\*, spin coherence time using Hahn echo technique T2, spin coherence time using CPMG pulse sequence technique T2 CPMG.

### Working schedule:

#### Designing initial version of reflectometry setup: sample holder, readout circuit, instrumentation setup

**Sample holder**

One of the key measurement requirements is to lower charge particles thermal energy to be able to resolve energy level splitting needed for confining one particle spin. For that reason it needs to be cooled down to low temperatures. In our case it is 4 Kelvin (K) or below. For the initial version of measurement system 4 K dewar with liquid helium has been used.

Double quantum dots samples are grown on silicon wafers and then cutted in 5x5 mm pieces. They need to be dipped into the liquid helium dewar for cooling. For this purpose Plexiglas sticks, were used. Sample was positioned on the bottom of the stick on the so called sample holder. Since, electrical signals needs to be delivered and afterwards measured from the sample, sample holder is done as printed circuit board (PCB) which routes all the electrical signals to and from the sample. From the room temperature instruments DC electrical signals are sent through the low thermal conductive twisted pair wires finishing in PCB connector and radio frequency signals are sent through coaxial cables. From PCB DC connector, DC signals are low pass filtered with on PCB RC filters to reduce thermal noise in the wires, as shown in Figure 4. After low pass filtering DC signals are routed to the gold plated bonding pads around area in the middle of the PCB (sample area) on which 5x5 mm sample is glued with silver paste (Figure 4). Electrical contacts to the DQD structure on the sample are achieved by wedge wire bonding technique from PCB bonding pads to the sample bonding pads electrically connected to the DQD gates. RF coaxial lines are finishing on the PCB mounted SMP connectors. After SMP connector, using bias tee, DC signal is added to the RF signal. From there signal is routed to the PCB bonding pads. SMP connectors and bias tees can be seen on Figure 4. Further these signals are connected to DQD gates with the same wedge wire bonding technique.

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Figure 4: Initial version of the PCB sample holder. Up is top and down is a bottom view of the PCB.

**Readout circuit**

To measure the charge state of the nanowire single electron transistor, ohmic reflectometry technique was applied. For that purpose RF signal was sent down the coax line (Figure). Reflected portion of that signal from the resonator circuit depends on the single electron transistor charge state. Working principle of ohmic reflectometry can be found at the end of the “State of the art” chapter. Resonator circuit was consisted of matching circuit (Figure 4) and single electron transistor resistance RS in parallel to parasitic capacitance CS, as can be seen in simple circuit model in Figure 3. Parasitic capacitance is capacitance to the ground that comes from bonding wires, sample itself, RF line and inductor.

(*There is nice circuit schematic in the Natalia paper. Since she is not explicitly telling that lowering parasitic capacitance increases sensitivity, I was thinking, maybe it would be good to take that circuit model with a reference and make a simulation in Qucs showing that with lowering parasitics change in reflection coef increases. For the purpose of justifying lowering parasitic capacitance by removing grounds in the PCB*)

For the purpose of minimization of this parasitic capacitance and thus increase sensitivity of the reflectometry, PCB ground plane is removed below RF lines, corresponding PCB bonding pads and a sample.

*Sample holder reflectometry LC circuit – how Cp is minimized and why it need to be minimized, some reference. RF 4K stick with amplifier and directional coupler.*

1. Germanium nanowire based, hole spin single quantum dot tuning and characterization with initial version reflectometry setup

*Put comparison reflectometry vs current measurement on Hannes sample (diamond graphs)*

1. Second generation of the reflectometry setup – *dil fridge, UHFLI, AWG, QTLab, new PCB (pict of Iron Man), additional DC filtering, low conducting NbTi coax with attenuators (pict of the probe).*

***TO DO:***

1. Moving to the gate reflectometry – *Adapting existing setup (readout circuit) for gate reflectometry, main points about gate reflectometry (from Hypoteses, look [12]), our sample considerations: gate coupling to the QD, comparison with [12]*
2. Optimizing (boosting) reflection parameter Γ regarding to: sample holder RF design, readout circuit configuration

Sample holder RF design – achieving small parasitic capacitance by engineering sample holder (PCB), achieving good 50 Ω on PCB RF lines and distributing them for achieving frequency division multiplexing

Readout circuit optimization – choosing appropriate inductor values L (Figure 3) while keeping parasitic capacitance small like stated above, optimizing directional coupler, amplifiers and filters configuration

1. Implementing setup for spin manipulation measurement
2. Measuring relaxation time
3. Spin dephasing time experiment
4. Spin coherence time experiment:
   * + 1. Hahn echo
       2. CPMG pulse sequence

### Innovative aspects:

In our group we are working with a **germanium nanowire based hole spin** double quantum dot. While other groups work with structures based on electron spin in gallium arsenide, electron spin silicon and Si:P and hole spin in silicon, this particular approach is not yet investigated. It has promising theoretical proposals *(put in which proposals and some numbers maybe)* in terms of qubit spin state manipulation and coherence time. Easy and fast spin state manipulation is expected because of in situ present **large spin orbit coupling** for heavy holes in Ge which enable **fast spin manipulation** by applying oscillatory electric field to particular qubit gates (Figure 2) eliminating necessity for oscillatory magnetic field. This means reducing fabrication complexity because nothing else is required except of already defined gates. Together with all the fabrication reduction complexity brought by gate reflectometry (as explained in *Definition of the problem*) our approach has high chances of **addressing scalability issue**.

**Relatively Long coherence time** is expected because of, before mentioned, low qubit charge spin coupling to the surrounding Ge and Si nuclei spin (**low hyperfine interaction**).

Gates on our DQD system (Figure 2) are positioned directly on the top of the nanowire in which quantum dots are formed. This implies **high capacitive coupling between gate and quantum dots**. This further implies **high sensitivity thus speed of gate reflectometry**, as explained in *Research methods*.

### International collaboration:

We are collaborating with spin qubit team in Charles M. Marcus laboratory in Copenhagen, lead by **Ferdinand Kuemmeth**. Since they are mature group with a big knowledge in instrumentation and spin qubits in overall, this collaboration helps us a lot in setting up our measurement setup. It would be helpful to visit them several times throughout the year. Here I would like to ask for the finances to cover the trip and accommodation costs for that purpose. The other significant collaboration is with **J.J. Zhang** in Beijing, China. He is material scientist providing us with silicon germanium nanowire samples.

### Overall goal of the project:

To implement one of the Loss and DiVincenzo’s criteria:

* **strong quantum measurements**,

and conducting **experiments of spin manipulation**.

Strong quantum measurements can be achieved by implementing gate reflectometry in our type of qubit structures. After having state readout solved, spin manipulation experiments can be done by applying bursts of microwave signal on electrostatic gates *(as explained in research methods).*

Spin manipulation experiments will be guideline for achieving second of the Loss and DiVincenzo’s criteria:

* accurate quantum gate operations

## Specific aims

### Clear aims:

Samples are done in cleanroom… *(take from someone in group)*

All experiments are done on DQD and TQD samples placed on the printed circuit board (PCB) sample holder *(put the picture)* in the dilution refrigerator with a base temperature of 10 mK.



Fig. x1. PCB holder (green) with mounted nanowire based sample (middle, grey) fabricated in our group by Lada Vukušić. Altogether mounted on golden plated copper fork on the dilution fridge insert. Copper wires are coaxial cables providing high frequency connection for spin manipulation and readout. Nanometer gates and ohmic contacts on the sample are connected by wedge wire bonding.

Electrical connection with the sample is achieved through thermally low conductive looms for DC signals and coaxial cables for RF and microwave signals. *(put the picture of the probe)* All cables finish in PCB connector and further electrical contact with the sample is achieved by wedge wire bonding.

On room temperature side there are several instruments for sending and receiving the signals from the sample. Firstly, DQD and TQD needs to be tune in correct electrostatic configuration what is achieved through the low-noise, optically isolated, voltage DC sources.

Sequences of high-speed pulses (ranging from hundreds of nanoseconds to several milliseconds) coordinated together with bursts of microwave signals (several GHz up to several tens of GHz) are sent via coaxial cables to manipulate DQD and TQD charge and spin state thus **providing spin qubit manipulations**.

Pulses are generated by arbitrary waveform generator (Tektronix AWG5014C) and microwave signals by microwave signal source (Rohde & Schwarz SMF100A).

**Qubit state is read-out** by probing radio-frequency (RF) signal reflected from resonant circuit consisted of discrete inductor and capacitor and gate capacitance between DQD and TQD top gates and confined charge area in those. Probing is done by high frequency lock-in measurement technique using Zurich Instruments UHFLI lock-in amplifier.

### Hypoteses:

*(Don’t know what to put here and what in research metodology)*

Main hypotheses is that our gate reflectometry is sensitive enough to achieve fast quantum state readout. Read out parameter (one which needs to be boosted) by gate reflectometry is resonance frequency shift ∆f due to hole tunneling form one to another dot in DQD or TQD system: . Resonant frequency, , of resonance circuit depend on externally added lumped inductance L which is externally added, and parasitic capacitance Cp. Because L is easily tunable and Cp can be reduced to some level by engineering, main hypotheses is that quantum capacitance due to a hole tunneling, CQ is big. It is given by our sample and we expect it to be relatively high because of the following reasons.

*(This need to be changed according to Csigma)*

CQ depends on capacitive coupling of reflectometry readout gate to QDs in a qubit Cg, and parasitic capacitances Cp, according to:

Previous expression suggest that pathway for boosting sensitivity of gate reflectometry is to have Cg high and Cp low.

Since in our types of structures gates are positioned on the top of the nanowire (d is small, l and w are relatively large) consisting QDs (Fig 1.) we expect high Cg ,according to:

Small parasitic capacitance we are going to achieve by engineering our sample holder (PCB). Isolating PCB sample area from the ground by removing ground planes and decoupling RF and DC ground by putting relatively large resistors in DC line around that area. On Fig.x.1. around the sample PCB is translucent indicating that there is no copper ground plane.



Figure 1. Nanowire based single quantum dot, predecessor of double quantum dot on Fig.x.

## Research methods

Here we are proposing integration of two qubit Loss and DiVincenzo’s criteria in our type of qubit. First is **qubit state (spin) readout**. Other one is **spin state manipulation**.

### Qubit state readout:

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Figure 2. Gate reflectometry schematic on the DQD sample from Fig.x1. LC resonators are connected to three of the gates. Signal from different gates are distinguished by frequency multiplexing since resonant frequencies are different because of different inductor values.

**What is reflectometry?**

Reflectometry is readout technique based on change of wave reflection coefficient Γ. It comes from electromagnetic wave principle – if the wave is travelling in media with impedance Z0  (e.g. coax cable) and it encounters change of impedance (e.g. coax end) to Z, portion of the wave will be reflected back according to the expression: , where Ar is amplitude and ᵠ( Ar) phase of the reflected, and Ain amplitude and ᵠ(Ain) phase of incoming wave. Reflection coefficient phase is ᵠ(Γ).

Putting resonant circuit with incorporated device instead of coax cable end one can measure change in impedance (capacitance) of that device. If elements of a resonant circuit – inductance L and capacitance C are properly chosen, on the resonant frequency of that circuit, , wave reflection coefficient Γ is minimized and it’s phase has inflection point and highest slope, Fig 2. top right blue and red.

In case of resonant LC circuit consisted of just L and C with very small R, Z is almost purely imaginary consisting of inductive and capacitive reactance. Thus if capacitance of sensed device changes -> ᵠ(Γ) changes and so phase of reflected wave ᵠ( Ar). Thus, by measuring phase of reflected wave ᵠ( Ar) and comparing it with ᵠ(Ain) one can get information of the impedance (capacitance) of sensed device.



Fig 3. S11 parameter vs frequency for different capacitors *(put something from qucs instead of this one)*

**Our plan:**

RF wave (tens to hundreds of MHz) is generated and sent from UHFLI out port down the coax cable. Going through directional coupler and encountering three resonant circuit frequency multiplexed on different resonance frequencies by choosing different values for surface mount inductors L1, L2, L3. Each of this inductors will be wire bonded to finger like gates, as shown in Fig 2. Here is an example for nanowire, double quantum dot based qubit. Gates LP (left plunger) and RP (right plunger) are capacitively coupled to the left and right quantum dot respectively. When electron undergo tunneling between the dots there is an onset of quantum capacitance, changing overall capacitance seen by the resonant circuit, which changes resonance frequency (according to expression for f0) and consequently amplitude and phase of reflected wave which is then measured.

### Spin state manipulation:

*Write something about it*

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